



FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEINFORMATION DISCLOSURE
STATEMENT BY APPLICANTSATTY. DOCKET NO.
174/308APPLICATION NO.
10/796,502APPLICANTS
David Mendel et al.CONFIRMATION NO.
3014FILING DATE
March 8, 2004GROUP ART UNIT
2185

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
MJB	6,407,576	6/18/02	Ngai et al.	326	41	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
MJB	Jason H. Anderson and Farid N. Najm, "A Novel Low-Power FPGA Routing Switch" (2004) (unpublished, submitted to the 2004 IEEE Custom Integrated Circuits Conference, Orlando, Florida, October 3-6, 2004).
MJB	Jason H. Anderson et al., "Active Leakage Power Optimization for FPGAs", 2004 ACM/SIGDA Twelfth International Symposium on Field Programmable Gate Arrays, Monterey, California, pp. 33-41 (February 22-24, 2004).
MJB	Jason H. Anderson and Farid N. Najm, "Low-Power Programmable Routing Circuitry for FPGAs" (2004) (unpublished, submitted to the 2004 International Conference on Computer Aided Design, San Jose, California, November 7-11, 2004).
MJB	Deming Chen and Jason Cong, "Low-Power Technology Mapping for FPGA Architectures with Dual Supply Voltages", 2004 ACM/SIGDA Twelfth International Symposium on Field Programmable Gate Arrays, Monterey, California, pp. 109-117 (February 22-24, 2004).
MJB	A. Gayasen et al., "Reducing Leakage Energy in FPGAs Using Region-Constrained Placement", 2004 ACM/SIGDA Twelfth International Symposium on Field Programmable Gate Arrays, Monterey, California, pp. 51-58 (February 22-24, 2004).
MJB	Fei Li et al., "Low-Power FPGA Using Pre-defined Dual-Vdd/Dual-Vt Fabrics", 2004 ACM/SIGDA Twelfth International Symposium on Field Programmable Gate Arrays, Monterey, California, pp. 42-50 (February 22-24, 2004).

EXAMINER

/Michael Brown/

DATE CONSIDERED 02/09/2007

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicants.

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
MJB	Fei Li et al., "FPGA Power Reduction Using Configurable Dual-Vdd", 2004 Design Automation Conference, San Diego, California, pp. 735-740 (June 7-11, 2004).
MJB	Arifur Rahman and Vijay Polavarapuv, "Evaluation of Low-Leakage Design Techniques for Field Programmable Gate Arrays", 2004 ACM/SIGDA Twelfth International Symposium on Field Programmable Gate Arrays, Monterey, California, pp. 23-30 (February 22-24, 2004).
MJB	"Mercury Programmable Logic Device Family", Data Sheet, Version 2.2, Altera Corporation, pp. 17-28 (January 2003).

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